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# Biosensors and Bioelectronics Open Access

Wang C and Morizio J. Biosens Bioelectron Open Acc: BBOA-109.

DOI: 10.29011/BBOA-109. 100009

Research Article

# A 0.7V-Supply, 214nW-Power, 2.23μVrms-Noise Subthreshold Symmetrical Low Noise Amplifier for 16-Channel Analog Front End

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**Citation:** Wang C, Morizio J (2018) A 0.7V-Supply, 214nW-Power, 2.23μVrms-Noise Subthreshold Symmetrical Low Noise Amplifier for 16-Channel Analog Front End. Biosens Bioelectron Open Acc: BBOA-109. DOI: 10.29011/BBOA-109. 100009

**Received Date:** 21 December, 2017; **Accepted Date:** 10 January, 2018; **Published Date:** 16 January, 2018

## Abstract

This work presents a 0.7 V Subthreshold Symmetrical Low-Noise Amplifier (SSLNA) of 16-channel electroencephalogram analog front end. The SSLNA features a low supply voltage of 0.7 V, a low power dissipation of 214 nW, a direct current gain of about 38 dB and a bandwidth of from 0.25 Hz to 480 Hz. On the aspect of the noise, the input-referred noise is 2.23 μVrms and the noise efficiency factor is 4.85. All the transistors of this SSLNA operate in the subthreshold region. The SSLNA is designed and verified in a 0.13 μm CMOS process.

## Introduction

Recordings of the neural Electroencephalogram (EEG) signals from many locations of the brain are an important source of the information for studying the function of the brain and various neurological disorders [1,2]. Therefore, multichannel Electroencephalogram (EEG) seizure detection SoCs are widely adopted in medical practice and in research [3,4], but most of them have an obvious limitation-limited number (no more than 8) of channels, whereas the American Clinical Neurophysiology Association sets the minimum technical standard recommendation for pediatric EEG as16 channels with bipolar and referential montages [4].

These recordings occupy a frequency band of from 1 Hz to about 40 Hz and have the small amplitudes ranging from 0.5 μVp to 100 μVp [5]. Due to the small amplitudes, EEG signals need to be amplified before digitization. Thus, the Low-Noise Amplifiers (LNA) are needed in an EEG signal recording sensor. Usually, the input-referred noise of the LNAs should be less than 4 μVrms [6]. EEG monitoring is one application where designers have targeted microvolt even sub-microvolt input-referred noise over a designed signal band [5]. For low-bandwidth and low-noise applications, the front-end amplifier of the recording sensor presents a power-consumption bottleneck since its current draw is noise-limited and cannot be scaled with the low data-rate [7]. Therefore, the prior works to improve the energy-efficiency of LNAs includes chopper [8], inverter-based LNAs [7], and low-supply-voltage amplifier design reaching 1.2 V [1,6]. However, most of LNAs still struggles on the aspect of energy efficiency and power consumption.

Therefore, to further improve the energy-efficiency, this paper uses a low supply of 0.7 V to design a 16-channel EEG analog front end. Our Subthreshold Symmetrical LNA (SSLNA) decreases the power dissipation and maintains the other aspects comparable, via scaling the supply voltage to 0.7 V and keeping all the transistors operate in the subthreshold region. This paper is organized as follows. The topologies and analysis of the whole analog front end, the proposed SSLNA and the other circuits are presented in Section II. The results are stated in Section III. Finally, the conclusions are given in Section IV.

## Topology

### Analog Front End Topology

The whole analog front-end topology is shown in Figure 1. It consists of the proposed sampling and processing amplifiers for 16 channels, a 16:1 multiplexer, an 8-bit modified flash ADC, a CMOS reference and a clock tree. The EEG signals are filtered by High-Pass Filters (HPF) and then processed by proposed SSLNAs. Then, the corresponding channel is chosen by one multiplexer to transfer one SSLNA output to a modified flash ADC. Then the

flash ADC converts the analog signal to digital signals. Moreover, the CMOS reference provides the bias current and voltage.

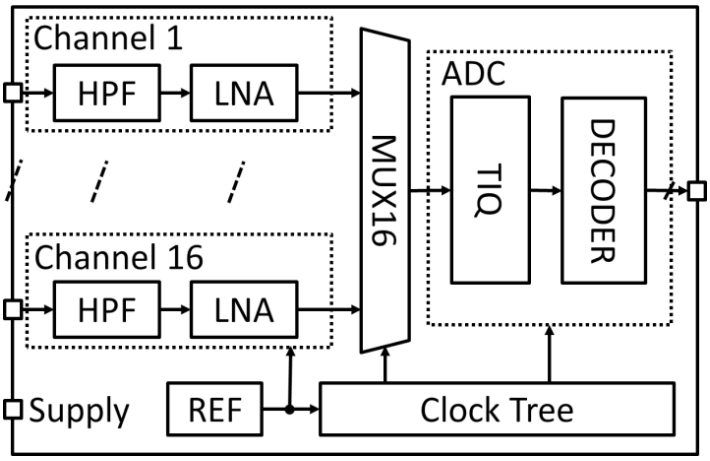



**Figure 1:** Analog front end topology.

## Proposed Subthreshold Symmetrical LNA

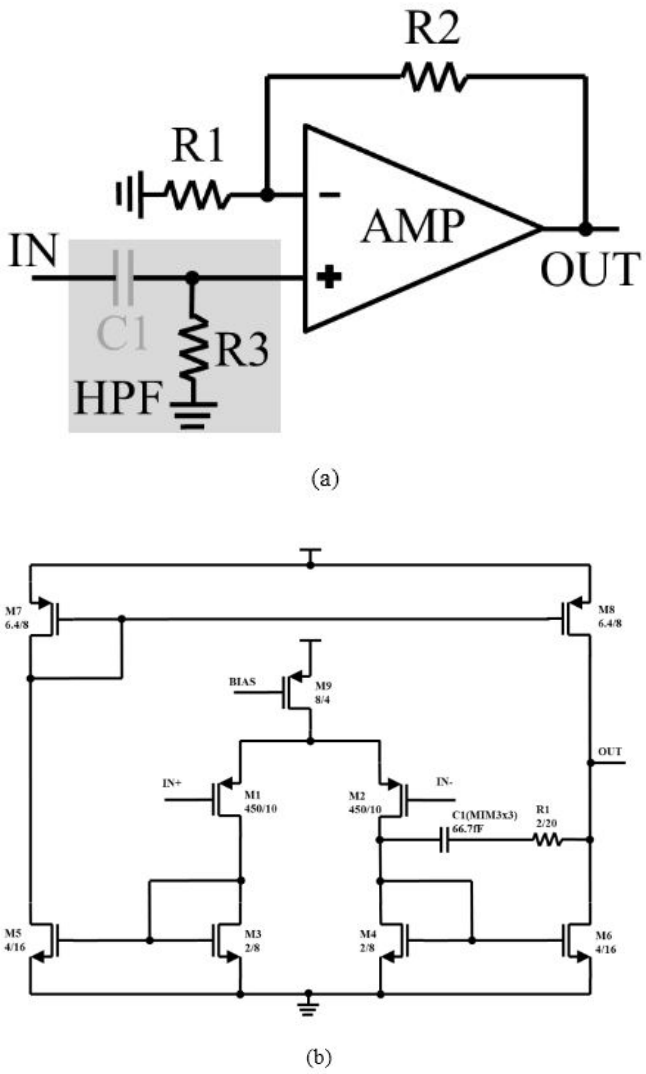
As shown in Figure 2a each channel has one HPF and one closed-loop SSLNA. It's easy to obtain the transfer function $G_{HPF}$ of HPF and the gain $A_{gain}$ of closed-loop SSLNA as the followings

$$G_{HPF} = \frac{R_3 C_1 \cdot s}{R_3 C_1 \cdot s + 1}$$

$$A_{gain} = \frac{R_2}{R_1} + 1$$

where $R_3$ is the filter resistor, $C_1$ is the filter capacitor, and $R_1$ and $R_2$ are the gain resistors. Noting that, the high pass frequency and closed-loop gain should respectively be around 0.3 Hz and around 40 dB for EEG signals.

Figure 2b shows the SSLNA. The SSLNA is based on a common symmetrical OTA but works at a low supply of 0.7V. It consists of one differential pairs implemented by the transistors M1 and M2, three pairs of current mirrors M3-M5, M4-M6 and M7-M8, a bias current M9, as well as the miller compensation C1 and R1 keeping the SSLNA stable.




**Figures 2(a,b):** Closed-loop SSLNA, (b) subthreshold symmetrical LNA.

Due to the transistors working in the subthreshold region, the drain current of the transistors should be

$$I_D = I_{D0} \frac{W}{L} e^{qV_{gs}/(ak_BT)} \left(1 - e^{-qV_{ds}/(k_BT)}\right)$$

where $I_{D0}, W, L, V_{gs}, V_{ds}, q, a, k_B$ and $T$ are the basic drain current, channel width, channel length, gate-source voltage and drain-source voltage, electron charge, the ration of the sum of oxide and depletion capacitances to oxide capacitance, Boltzmann constant and temperature, respectively. $I_{D0}$ and $a$ can be expressed as

$$I_{D0} = \mu C_{OX}(a-1)\left(\frac{k_B T}{q}\right)^2 e^{-qV_{th}/(ak_B T)}$$

$$a = \frac{C_{OX} + C_{depl}}{C_{OX}} \approx 1.5$$

where $C_{OX}$, $C_{depl}$, $\mu$ and $V_{th}$ are the oxide capacitance per unit area, depletion capacitance, carrier mobility and the threshold voltage, respectively.

According to the OTA principle, the gain and bandwidth can be easily written as

$$A_{dm} = g_{mg}(r_{oN} \| r_{oP})$$

$$BW = \frac{1}{2\pi(r_{oN} \| r_{oP})C_{OUT}}$$

where $C_{OUT}$ is the capacitance of node OUT, $r_{oN}$ ($r_{oP}$) is the equivalent resistance of M8 (M6) and $g_{mg}$ is the transconductor of M1 or M2. The transconductor $g_{mg}$ and the equivalent resistance $r_o$ can be calculated as

$$g_{mg} = \frac{\partial I_D}{\partial V_{gs}} = \frac{qI_D}{ak_B T}$$

$$r_o = 1\Big/\frac{\partial I_D}{\partial V_{ds}} \approx 1\Big/\left(\frac{q}{k_B T} \cdot e^{-qV_{ds}/(k_B T)} \cdot I_D\right)$$

Therefore, via substituting $g_{mg}$ and $r_o$ into and bandwidth $BW$, it's easy to find the following

$$BW \leftarrow \left(\frac{W_6}{L_6}, \frac{W_8}{L_8}\right)$$

Noting that, the target of the bandwidth i.e. a low pass frequency is around 500 Hz for EEG signal.

Due to all the transistors operating in the subthreshold region reduce the ultra-low power, and hence the root mean square (rms) voltage of the input mosfet at the frequency band of from $f_1 f_1$ to $f_2$ is express as [9]

$$\bar{v}_{gate}^2 = \frac{2nk_B T}{g_{mg}}\left((f_2 - f_1) + f_c \cdot ln\left(\frac{f_2}{f_1}\right)\right)$$

where $f_c$ is the crossover frequency which can be written as

$$f_c = \frac{g_{mg}\, a}{WLC_{OX}} \frac{N_{ot}}{N^*}$$

where $N^* = \frac{nC_{OX}\varphi_t}{q}$, $N_{ot} = \frac{k_B T \cdot N_t(E)}{\gamma}$, $n$ is the slope factor slightly dependent on the gate voltage, $\varphi_t$ is the thermal voltage, $N_t(E)$ is the density of oxide traps per unit volume and unit energy and $\gamma$ $\gamma$ is the attenuation coefficient of the electron wave function in the oxide. For $N_t(E) = 4 \times 10^{16}\ cm^{-3}eV^{-3}$, $k_B T = 0.026eV$, $\gamma = 10^8\ cm$, and $N_{ot}$ is of the order of $10^7\ cm^2$.

Each transistor in the SSLNA introduces the approximate amount of noise versus their area, and the same number of effective traps for both nMOS and pMOS transistors is assumed [9]. Consequently, neglecting the common mode noise of the current source, the input referred noise can be estimated by simply timing the ratio of total and input mosfet areas with the rms voltage of input mosfet [9], as

$$\bar{v}_{input\_referred\_noise}^2 = \frac{W_{total}}{W_{input}} \bar{v}_{gate}^2$$

Therefore, via substituting $\bar{v}_{gate}^2$ into $\bar{v}_{input\_referred\_noise}^2$, it's easy to find the following

$$\bar{v}_{input\_referred\_noise}^2 \leftarrow \left(y_N = \sum_{i=1}^{9} W_i, \frac{W_{input}}{L_{input}} \frac{W_6}{L_6}, \frac{W_8}{L_8}\right)$$

Noting that, for EEG signals the input referred noise should be no more than 2.5 μVrms.

Furthermore, the noise efficiency factor can be defined [10] as

$$NEF = \bar{v}_{input\_referred\_noise} \sqrt{\frac{I_{tot}}{4\pi\sqrt{10} \cdot n(V_{gs} - V_{th})k_B T \cdot BW}}$$

where $I_{tot}$ is the total drain current in the SSLNA.

So, tuning the appropriate widths and lengths of the transistors in the proposed SSLNA can achieve the aforesaid targets. The chosen parameters of the transistors are shown in Figure 2b.

## Flash ADC

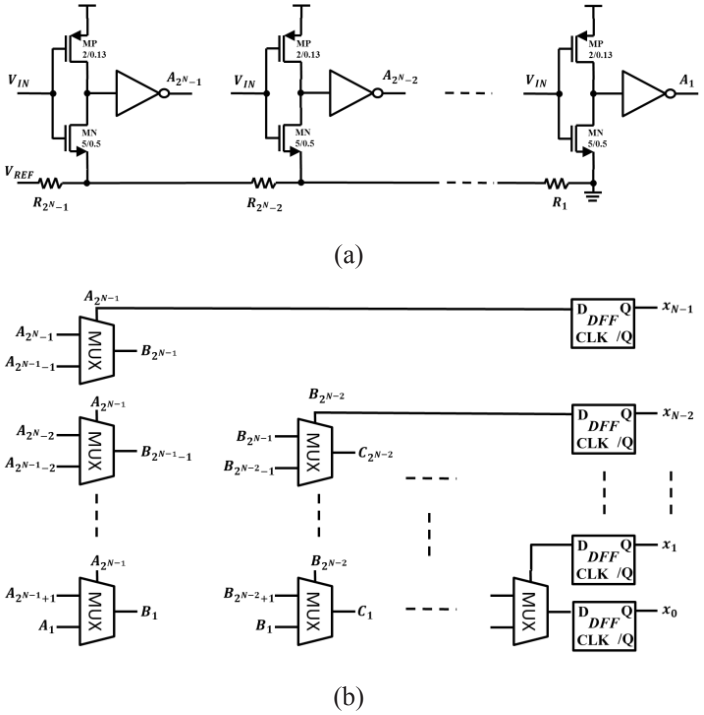
A $N$-bit modified Flash ADC is achieved combining Threshold Inverter Quantization (TIQ) and multiplexer-based decoder. TIQ based on a single NMOS comparator (consisting of a resistor and CMOS inverters) is transplanted to overcome the drawbacks of traditional comparator and TIQ based on two cascaded CMOS inverters. Traditional comparator requires a

large number of transistors causing the big chip area and power consumption. TIQ based on two cascaded CMOS inverters requires its $W/L$ ratios being increased up to maybe thousand times when the number of bits is increased. The chosen TIQ based on a single NMOS comparator is shown in Figure 3a [10]. The resistor is used to set the voltage between source and bulk $V_{sb}$, the first inverter is used to compare the input $V_{IN}$ and threshold voltage $V_{TH}$, and the second inverter is used to amend the comparison result. $V_{TH}$ of NMOS can be expressed as

$$|V_{TH}| = |V_{TH0}| + |V_{TH0}|\left(\sqrt{2\varphi_f + |V_{sb}|} - \sqrt{2\varphi_f}\right)$$

where $V_{TH0}$ is threshold voltage when source and bulk is connected, $V_{TH0}$ is body effect parameter, $\varphi_f$ is semiconductor parameter. So $V_s$ can be biased and adjusted by the series resistors to attain reference voltage. The NMOS operating mechanism depended on the relationship of $V_{gs}$ and $V_{TH}$. If $V_{gs} < V_{TH}$, NMOS is at the "cut-off" region, there is no current flowing through NMOS and it will output a negative logic "0". Otherwise, NMOS is at the "ON" region (whether in non-saturation or saturation), $V_{out} = V_s + I_D \cdot R_{MOS}$ and it will output a positive logic "1". Obviously, $W/L$ ratio of NMOS transistor need be chosen to make a good trade-off between input range and area, thus we use $5\ \mu m/0.5\ \mu m$.

Multiplexer based decoder is used to overcome the disadvantages of ROM, Wallace tree and folded decoders. ROM decoder is slow and power consuming. Wallace tree decoder and folded decoder require a larger length of critical path which is approximately third and twice of multiplexer-based decoder, respectively. The used multiplexer-based decoder is shown in Figure 3b. For an $N$-bit flash ADC, the Most Significant Bit ($MSB$ ) of the binary outputs is high if more than half of the outputs in the thermometer scale are logic one. Hence $MSB$ is $A_{2^N-1}$. To find the second most significant bit ($MSB-1$) of the original thermometer scale is divided into two partial thermometer scales, separated by $A_{2^N-1}$. The partial thermometer scale to decode is chosen by a set of 2:1 multiplexers, where the previous decoded binary outputs are connected to the control input of the multiplexers. $MSB-1$ is then found from the chosen partial thermometer scale in the same way as $MSB$ was found from the full thermometer scale. Similarly, all the $N$ bits can be obtained. In general, the decoder requires 2:1 multiplexers with a number of $y_N = \sum_{q=1}^{N-1}(2^{N-q}-1)$, and the critical path in units of $t_{MUX}$ is $N-1$.




**Figures 3(a,b):** TIQ with a single MOS comparator, (b) multiplexer based decoder.

Usually, the signal-to-noise rate (SNR) of ADC is defined as

$$SNR = 20log\left(\frac{noise\ value}{input\ range}\right) = 20log\left(\frac{v_{in\_noise\_ADC} + \bar{v}_{ther\_noise\_ADC}}{V_{ADC_{range}}}\right) \approx 20log\left(\frac{6.6 \cdot A_{gain} \cdot \bar{v}_{input\_refferred\_noise}}{V_{ADC_{range}}}\right)$$

where $v_{in\ noise\ ADC}$ is the peak value of ADC input noise, $\bar{v}_{in\_noise\_ADC}$ is the rms value of ADC input noise, $R_{ADC}$ is the total resistance of ADC and $V_{ADC\_range}$ is the input range of ADC which is around 0.5V. Therefore, using the targets in last subsection, it is estimated that $SNR \approx 49.63\text{dB}$.

Besides, the relationship of SNR and ADC accuracy $N$ can be express as

$$SNR = 6.02N + 1.76$$

Thus, to make $SNR \geq 49.63\text{dB}$, the modified flash ADC requires its accuracy meeting $N \geq 7.952$. Therefore, our flash ADC has 8 bits.

## CMOS Reference

This paper transplants a CMOS reference structure [12,13] shown in Figure 4 to 0.13μm CMOS process. A self-biasing circuit (M1, M2, M3 and M4) and MOS resistor M5 generates the

reference current $I_p$. The transistor M7 and two source-coupled pairs (M6 and M9, M8 and M10) generates the reference voltage $V_{REF}$. Via adjusting the aspect ratios of the transistors, the zero TC principle of CMOS reference is derived as

$$V_{REF} = V_{TH0} + C$$

where $C$ is a parameter which is dependent on process, but not on the temperature. More details can be seen in Refs. [12, 13].

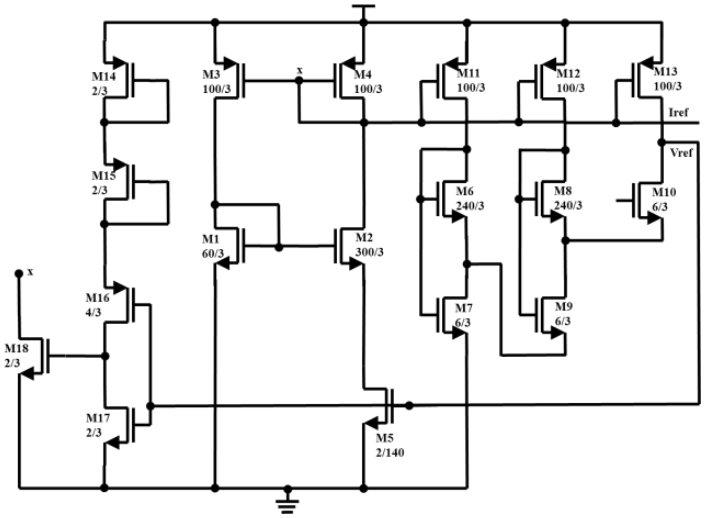



**Figure 4:** CMOS reference.

## Clock Tree

The ring oscillator, which uses an odd number of the inverters to give the effect of a single inverting amplifier with a gain of greater than one, is used as the basic clock generator. If $t_{INV}$ represents the time-delay of a single inverter and $n_{INV}$ represents the number of inverters, the frequency is given by $f_{clock} = \frac{1}{2 \cdot t_{INV} \cdot n_{INV}}$. Then a series of D flip flops are used as the even frequency dividers. The number of the inverters is chosen as three to reduce area, power consummation and design complexity. Thus, the clock tree is obtained as shown in Figure 5.

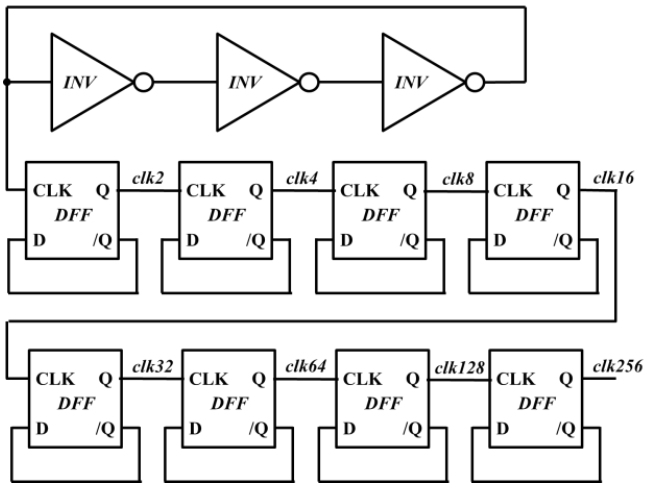



**Figure 5:** Clock tree.

# Results and Comparisons

## Simulation Results

Figure 6 shows the frequency response of one channel with HPF and closed-loop SSLNA. It can be seen that it has a low-frequency gain of about 38 dB, a bandwidth of about 0.25~480 Hz and a phase margin of about 61°.

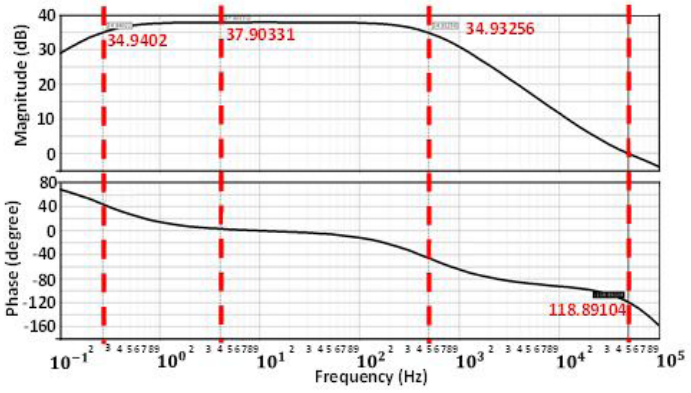



**Figure 6:** Frequency response.

The noise spectrum from 0.1 Hz to 100 kHz is shown in Figure 7. The Input-Referred Noise Voltages (IRNV) in the range of 0.1~480Hz are about 2.23 $\mu V_{rms}/\sqrt{Hz}$ and the corner frequency is about 300 Hz. The Noise Efficiency Factor (NEF) is calculated as 4.85. Obviously, the gain, bandwidth and noise voltage meet the targets set for EEG signals in Sec. II. That is to say, even at a low supply of 0.7V increasing the total widths of all the transistors and adjusting the ratios of width to length can achieve the low noise, meanwhile, maintain appropriate gain and bandwidth.

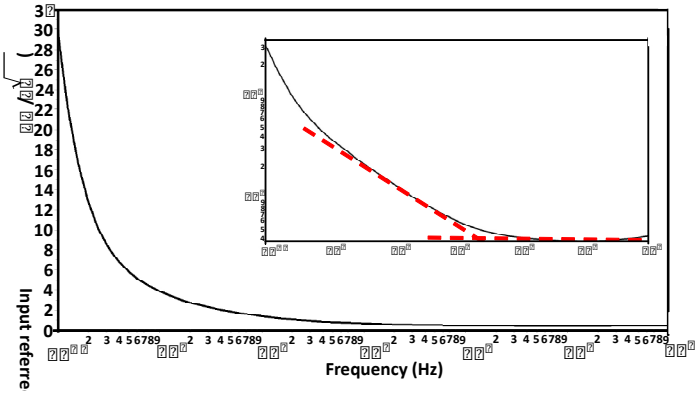



**Figure 7:** Noise spectrum.

A sinusoidal signal with a frequency of 10 Hz and an amplitude of 1 mV is sent to SSLNA configured as unit gain. It can be seen from Figure 8 that the Dynamic Range (DR) between the fundamental frequency and 3rd harmonic is 90 dB and the Total Harmonic Distortion (THD) is 0.25%.

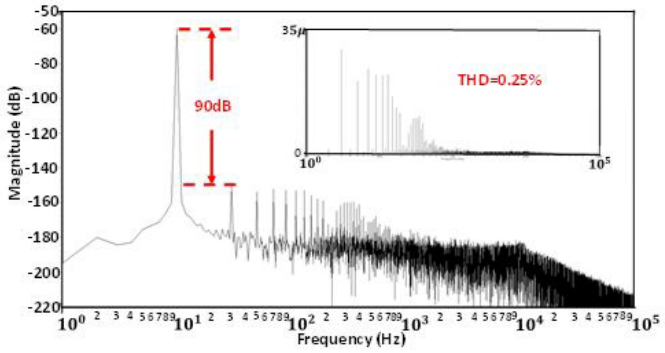



**Figure 8:** Dynamic range and THD.

The slew rate is bigger than 2500 V/s as shown in Figure 9.

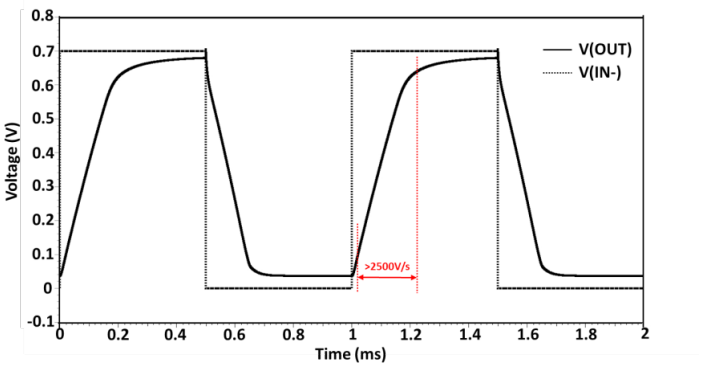



**Figure 9:** Slew rate.

From Figure 10 the output swing is from 0.1 V to 0.65 V and the Input Common Mode Range (ICMR) is from 0.09 V to 0.65 V.

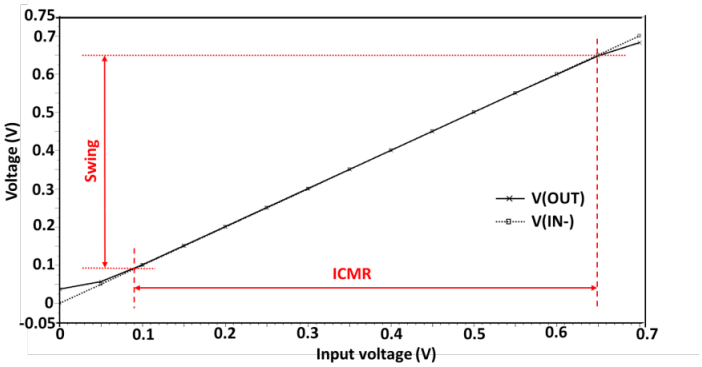



**Figure 10:** Output swing and input common mode range.

As shown in (Figure 11), SSLNA under closed-loop has a Common-Mode Rejection Ratio (CMRR) of about 78 dB and a power-supply rejection ratio (PSRR) of about 71 dB, which are sufficient for EEG signals.

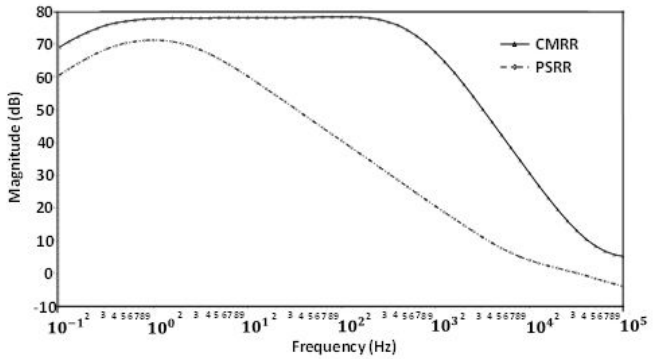



**Figure 11:** CMRR and PSRR.

Figure 12 and Figure 13 respectively show the power loss and layout graph of the analog front end implemented in a 0.13μm CMOS technology. On the aspect of power loss, the analog front end has a total loss of 12.65 μW including 214 nW from one SSLNA. On the aspect of layout area, it has a total dimension of 7.3×3 $mm^2$ including 1.6×0.4 $mm^2$ from one SSLNA, 0.5×0.26 $mm^2$ from one ADC and 0.13×0.26 $mm^2$ from the CMOS reference. To decrease the offset of SSLNA caused by fluctuation of ion density, each transistor is decomposed into even centrosymmetric transistors with half ratio.

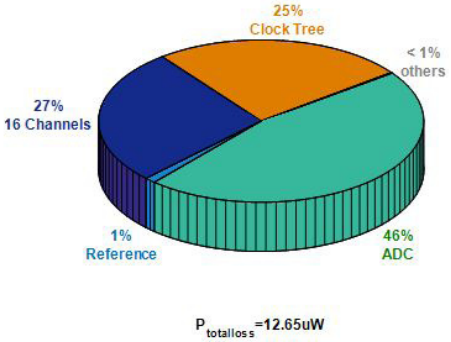



**Figure 12:** Power loss.

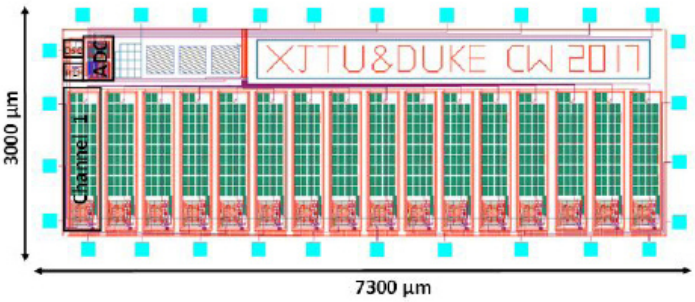



**Figure 13:** Layout.

## Comparisons

BW, IRNV, NEF, THD, DR, SR, ICMR, CMRR and PSRR is bandwidth, input referred noise voltage, noise efficiency factor, total harmonic distortion, dynamic range, slew rate, input common mode range, common mode rejection ratio and power supply rejection ratio. The comparisons of the proposed SSLNA with recent LNAs are listed in Table 1. The SSLNA makes the supply voltage and power dissipation respectively smaller than 1 V and 250 nW, and also achieves the comparable other parameters with those of recent works. The bandwidth is 0.25~480 Hz is enough for the EEG recordings.

| Parameter | [1] | [6] | [7] | [14] | [15] | This work |
|---|---|---|---|---|---|---|
| Year | 2016 | 2015 | 2016 | 2014 | 2015 | |
| Process (μm) | 0.18 | 0.065 | 0.18 | 0.35 | 0.18 | 0.13 |
| Supply (V) | 1.2 | 1.2 | 0.2&0.8 | 2.5 | 1.8 | 0.7 |
| Power (μW) | 9.9 | 1.44 | 0.79 | 0.0825 | 90 | 0.214 |
| Gain (dB) | 52 | 34 | 57.8 | 40.7 | 45 | 38 |
| BW (Hz) | 1-5k | 11k | 670 | 100 | 3-2.5k | 0.25~480 |
| IRNV (μVrms) | 5 | 0.037 | 0.94 | 2.8 | 2.1 | 2.23 |
| NEF | 7 | 1.8 | 2.1 | 1.96 | 11 | 4.85 |
| THD (%) | 0.95 | N/A | N/A | 1 | N/A | 0.25 |
| DR (dB) | N/A | N/A | N/A | 53.43 | N/A | 90 |
| SR (V/s) | N/A | N/A | 300 | N/A | N/A | 2500 |
| Swing (mV) | N/A | N/A | 240 | N/A | N/A | 550 |
| ICMR (mV) | N/A | N/A | N/A | N/A | N/A | 560 |
| CMRR (dB) | 65 | 94 | 85 | >70 | N/A | 78 |
| PSRR (dB) | N/A | 100 | 74 | >70 | N/A | 71 |
| Area ($mm^2$) | N/A | None | 0.48 | 0.17 | 0.178 | 1.6×0.4 |

**Table 1:** Comparisons of SSLNA with recent LNAs.

## Conclusion

This work presented a successful design and validation of a Subthreshold Symmetrical Low Noise Amplifier (SSLNA) of 16-channel analog front end for electroencephalogram signals in a 0.13 μm CMOS process. The SSLNA features a low supply voltage of 0.7 V, a low power dissipation of 214 nW, a direct current gain of about 38 dB and a bandwidth of 0.25~480 Hz. Besides, the input-referred noise voltage is 2.23 μVrms and the noise efficiency factor is 4.85. Moreover, the SSLNA has a dynamic range of 90 dB and a total harmonic distortion of 0.25% for a sinusoidal input with the frequency of 10 Hz and the amplitude of 1 mV. Besides, CMRR and PSRR respectively are 78 dB and 71 dB.

## Acknowledgment

This project is sponsored by the corporate gift donations to the VLSI Design Center at Duke ECE Department under Dr. James Morizio's direction and the China Scholarship Council under grant no. 201506280038.

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