OPEN ACCESS

GAVIN PUBLISHERS

Biosensors and Bioelectronics Open Access

Review Article

Al-Absi MAK. Biosens Bioelectron Open Acc: BBOA-121.

DOI: 10.29011/BBOA-121. 100021

A New Compact and Tunable CMOS Temperature Sensor

Munir A. Kulaib Al-Absi*

Department of Electrical Engineering, King Fahd University of Petroleum & Minerals, Saudi Arabia

***Corresponding author:** Munir A. Kulaib Al-Absi, Associate Professor, Department of Electrical Engineering, King Fahd University of Petroleum & Minerals, Dhahran 34463, Saudi Arabia. Tel: +96638603696; Fax: +96638603535; Email: mkulaib@kfupm.edu.sa

Citation: Al-Absi MAK (2018) New Compact and Tunable CMOS Temperature Sensor. Biosens Bioelectron Open Acc: BBOA-121. DOI: 10.29011/BBOA-121. 100021

Received Date: 10 January, 2018; **Accepted Date:** 02 March, 2018; **Published Date:** 09 March, 2018

Abstract

This paper presents a new compact low voltage and low power CMOS integrated temperature sensor for ultra-low power applications. The design is based on cross-coupled MOS transistors operating in the subthreshold region. The new sensor is a negative resistance that varies with temperature and hence it can be used to sense and amplify the signal at the same time. The functionality of the design was confirmed using Tanner T spice in 0.18µm CMOS TSMC process technology. The circuit is operated from ±0.5Volt and consumes 120nW.

Index Terms: Cross-Couple; Integrated Temperature Sensors; Negative Resistance; Subthreshold

Introduction

Temperature sensors are widely used in various applications such as wireless sensor networks, Radio Frequency Identification (RFID), automotive systems, microprocessors, DRAM, and energy harvesting systems, Moreover, temperature sensors are needed to monitor the thermal profile of the integrated chip because the temperature affects the performance such as speed, power, and reliability. This fact made the temperature measurement and control mandatory [1-6]. There are many sensors design techniques available in the literature. However, emerging technology trends require the development of better sensors in terms of efficiency, low calibration cost and operation at low power supply voltage. The design in [1] is based on using two Op-Amps in addition to a reference generator. In [2] a temperature to pulse generator is used in which two lines are used along with exclusive OR gate. Reference [3] presents an accurate CMOS integrated temperature sensor. This design is complex and based on Proportional to Absolute Temperature (PTAT) source and bandgap reference. The design in [4] presents a bandgap temperature sensor and a temperature sensor based on the delay line. In [5] Substrate PNP transistors are used for temperature sensing and for generating the reference voltages which is almost the same concept as the design in [1]. In [6] a CMOS temperature sensor is presented. The design uses two Op-Amp buffers and large number of transistors to generate PTAT and Vref. In [7] a Resistor Temperature Detector (RTD)-based temperature sensor is presented. The design is based on using planner resistance temperature detector which can be manufacturer with microelectronics processing technique.

To my knowledge, there is no CMOS-based RTD sensor is available in the open literature. In this paper, a new compact low voltage and low power CMOS integrated temperature sensor is presented. The rest of the paper is organized as follows: Section II presents the proposed design and mathematical analysis. The simulation results and discussion are presented in section III. Section IV concludes the paper.

Proposed Temperature Sensor

The proposed design is based on the cross-coupled MOSFETs shown in (Figure 1). The two transistors are biased in subthreshold region. The drain current of MOSFET in subthreshold is given by [8]:

$$I_D = I_{DO}\frac{W}{L}e^{\left(\frac{V_{GS}-V_{TH}}{nV_T}\right)} \quad (1)$$

Where I_{Do} is the saturation current, n is the slope factor and

V_T is the thermal voltage? To keep the MOSFETs operating in the sub-threshold forward saturation region, the following conditions must be satisfied:

Where I_Do is the saturation current, n is the slope factor and V_T is the thermal voltage? To keep the MOSFETs operating in the sub-threshold forward saturation region, the following conditions must be satisfied:

$$\frac{I_{DO}}{I_D} << 1 \text{ and } V_{DS} > 4V_T \quad (2)$$

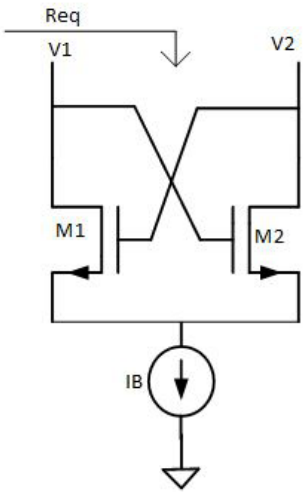


Figure 1: Proposed design.

Using the small signal equivalent circuit, with M1 and M2 match transistors, it is easy to show that the equivalent resistance seen between nodes V1 and V2 is given by:

$$R_{eq} = -\frac{2r_o}{1+g_m r_o} \quad (3)$$

In subthreshold region, $g_m = \frac{I_D}{nV_T}$, and $r_0 = \frac{1}{\lambda I_D}$, this implies that $g_m r_0 >> 1$ and equation (3) can be written as :

$$R_{eq} = -\frac{2}{g_m} = -\frac{2nV_T}{I_B/2} = -\frac{4nK}{q}\frac{T}{I_B} \quad (4)$$

Where T is the temperature in Kelvin. It is clear that equation (4) implements a resistance-type temperature sensor whose resistance varies linearly with temperature. The sensitivity of the design can be tuned using the bias current I_B.

The circuit diagram for the proposed design is shown in (Figure 2). The bias current I_{B2}=0.5 I_B and is copied through MP2 and MP3 to assure same bias current is supplied to M1 and M2.

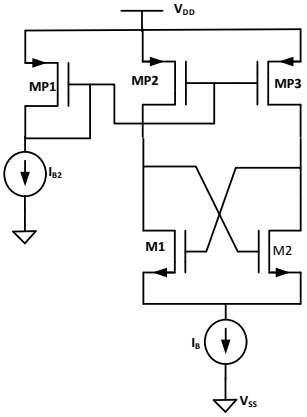
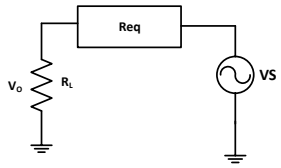


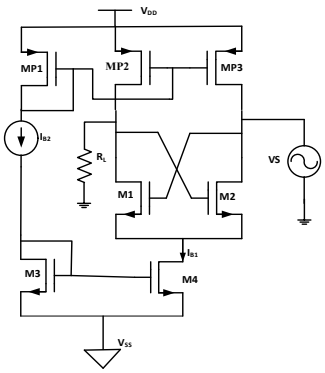
Figure 2: The circuit diagram of the proposed design.

Simulation Results

To prove the design concept, the proposed circuit was simulated using tanner T spice with 0.18µm TSMC CMOS process technology. The equivalent resistance is connected to an AC source with 20mV amplitude, 10KHz frequency and a 1Mega Ohm load resistor as shown in (Figure 3 a,b).



(a)



(b)

Figure 3(a, b): The circuit used for simulation.

The supply voltage V_{DD} =-V_{SS}=0.75V and the transistors dimensions are given in (Table 1). The bias current I_{B2} is set to 25nA and is doubled through the current mirror formed by M3-M4 by proper adjustment of channel width of M4. The dimensions of transistors M1-M3 are W=2µm and L=2µm, Mp1-Mp3 are W=5µm and L=2µm and for M4 W=3.852µm, L=2µm.

	This work	[1]	[3]	[6]	[7]
Techno logy(µm)	0.18	0.18	0.5	0.18	-
Sensitivity (tunable)	10000/°C	-	-	-	4.5 Ω/°C)
Temp. range (°C)	-50-150	0-100	-40-100	-40-100	0-150
Supply voltage(V)	±0.5	1.2	2.5-5.5	1-1.8	-
Power consum ption(nW)	120	71	350	2200	-
% of Relative inaccuracy	6	2.9	0.4	0.7	-
Area (mm)^2	0.006	0.09	0.55	0.517	-

Table 1: Performance comparison.

The temperature was varied from -50°C to 150°C, and the output voltage is given by:

$$V_o = V_s \frac{R_L}{R_L + R_q} \quad (5)$$

Plot of the calculated and simulated resistance as a function of the temperature is shown in (Figure 4). It is clear from the plot that the resistance varies from 2.5-to-4.5Mega ohm as the temperature varies from -50°C to 150°C. The relative error between the calculated and simulated results are shown in (Figure 5). It is evident from the plot that there is a deviation between the calculated and simulated values. One reason could be the fixed value of n used (n=1.5) in equation (4) for the calculated values of R_{eq}.

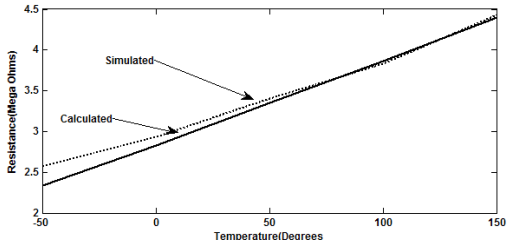


Figure 4: Plot of the simulated and calculated resistance VS temperature (I_{B1}=50nA).

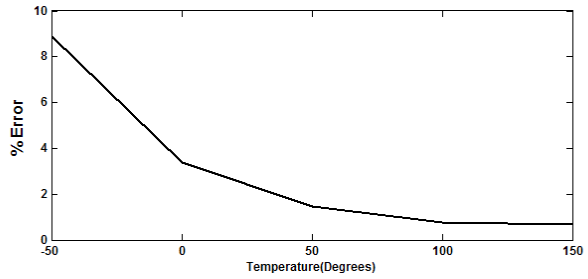


Figure 5: Plot of the relative error between calculated and simulated resistance (I_{B1} =50nA).

The bias current is set to 100nA and plot of the calculated and simulated resistances are shown in (Figure 6).

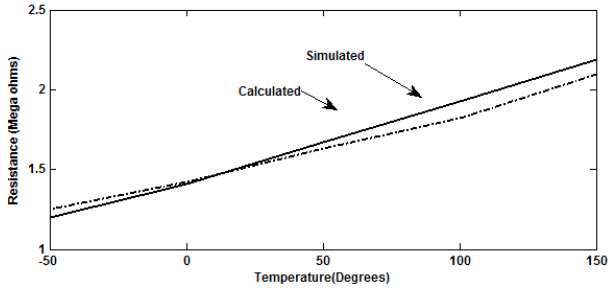


Figure 6: Plot of the simulated and calculated resistance VS temperature (I_{B1} =100nA).

It is clear from the figure the resistance is reduced to half its value and this agrees well with equation 4. The % relative error is less than that shown in (Figure 7).

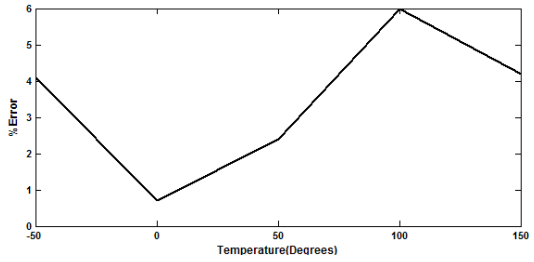


Figure 7: Plot of the relative error between calculated and simulated resistance (I_{B1} =100nA).

The circuit was simulated for transient response with I_{B1} =50nA, and 100nA. Simulation results are shown in (Figures 8,9) respectively. It is clear from the two figures that the circuit is functioning properly. Also, it can be seen that the output voltage in (Figures 8, 9) has 180° phase shift which indicates that the sensor resistance is negative and higher than R_L . Also, it is evident from figure 9, that the output voltage is higher than the input voltage and according to equation 5 this will happen only if the sensor resistor is negative.

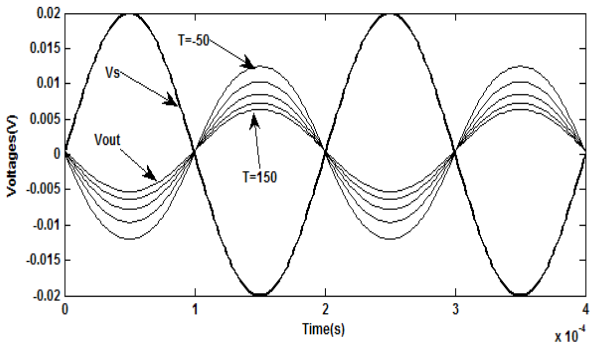


Figure 8: Transient response (I_{B1} =50nA).

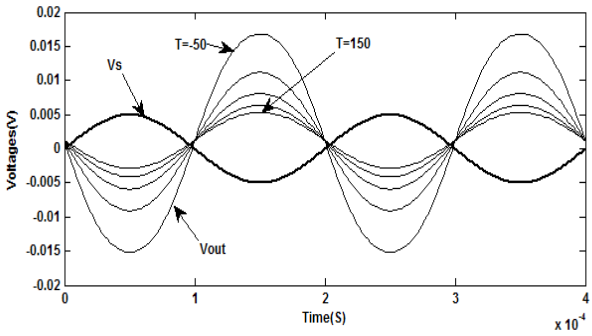


Figure 9: Transient response (I_{B1} =100nA).

Since the sensor is a negative resistance that varies with temperature, it can be used to amplify the signal at the same time as shown in (Figure 9). It must be noted that, increasing the bias current will drive the transistor out of subthreshold forward saturation and consequently will limit the input range. For I_{B1} =100nA, the input signal amplitude is reduced to 5mV to assure proper operating mode. Alternatively, one can increase the aspect ratios of all transistors so that higher biasing current can be used while keeping all transistors in forward saturation. The performance of the proposed design is compared to the existing temperature sensor and is summarized in (Table 1).

It is clear from (Table 1) that the proposed design is superior in terms of sensitivity, area, temperature range. However, the power consumption is higher than that in [1].

Conclusion

A new compact and tunable CMOS low voltage and low power tunable integrated temperatures sensor is developed. The sensor can be used in many applications where temperature monitoring is

crucial to minimize the power consumption especially in battery-powered circuits. The circuit is powered from ±0.5V DC supply and consumes 120nW.

Acknowledgement

The author would like to thank KFUPM for the support of this work. Thanks, are extended to Prof. Abuelma'atti for his valuable comments.

References

1. Jeong S, Foo Z, Lee Y, Sim JY, Blaauw D, et al. (2014) A fully-integrated 71 nW CMOS temperature sensor for low power wireless sensor nodes. IEEE J Solid-State Circuits 49: 1682-1693.
2. Kim HW, Ann SH, Kim NS (2016) CMOS Integrated Time-Mode Temperature Sensor for Self-Refresh Control in DRAM Memory Cell. IEEE Sens J 16: 6687-6693.
3. Li J, Weisheng X, Youlin Y (2010) Accurate operation of a CMOS integrated temperature sensor. Microelectronics J 41: 897-905.
4. Makinwa KAA (2010) Smart temperature sensors in standard CMOS. Procedia Eng 5: 930-939.
5. Pertijs MAP, Makinwa KAA, Huijsing JH, Santos M, Member SS, et al. (200) A CMOS smart temperature sensor with a 3 sigma; inaccuracy of plusmn;0.1/deg/C from -55/spldeg/C to 125/spl deg/C. IEEE J Solid-State Circuits 40: 2805-2815.
6. Xie L, Liu J, Wang Y, Wen G (2014) A low-power CMOS smart temperature sensor for RFID application. J Semicond. 35: 115002
7. Santos EJP, Ieee SM, Vasconcelos IB, Ieee M (2008) RTD-based Smart Temperature Sensor: Process Development and Circuit Design. Microelectronics 10071608: 11-14.
8. Wang A, Calhoun BH, Chandrakasan AP (2006) Sub-threshold Design for Ultra Low-Power Systems. Springer-Verlag, New York, NY, USA.